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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,573	10/23/2003	In-Duk Song	041993-5223	5961

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EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,573	SONG ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgement is made of papers filed claiming priority from Korean Patent Application No. P 2002 –087480 filed on December 20, 2002, which have been placed of record in the file and the presently the earliest filling date available is December 20, 2002.

Drawings

Figures 1 through 4 B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures.

If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

No IDS to date has been filed in this case.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 3 lines 11-13 recite, "..and to remain the photo resist layer of the first light transmission region " it is not understood what Applicants' intend to include/exclude by the recitation. (similar recitation in claim 10 also) .

Similarly claim 3 lines 14 to 19 recite," developing the etching the organic passivation layer to remove a part of the organic passivation layer of the second light transmission region; removing the photoresist layer; and etching the organic passivation layer to remove a remaining organic passivation layer." it is not understood what Applicants' intend to include/exclude by the recitation. What is meant by "developing the etching " etc.

Claims 4-5 and 11-17 are rejected at least for depending upon rejected claim 3 and 10 respectively.

Claims 6 and 14 recite, "the method of claim 1, wherein the forming a thin film transistor comprises, forming a gate electrode on the first substrate; insulating layer over the first substrate; depositing a gate forming a semiconductor layer on the gate insulating layer; and forming a source electrode and a drain electrode on the semiconductor layer. " it is not understood from the above recitation how the first recited step "forming a gate electrode on the first substrate" is related to the other steps mentioned e.g. depositing a gate forming a semiconductor layer. Further it is not understood what Applicants' intend to include/exclude by the recitation, " depositing a

gate forming a semiconductor layer on the gate insulating layer ". It is generally understood in the art that the gate (made of conductive material like a metal) is a separate layer from the semiconductor layer on which the gate is formed. It is not understood what Applicants mean by gate forming a semiconductor layer.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rho et al. (U.S. Patent NO. 6,597,415, herein after Rho) in view of Kim (U.S. Patent No. 6,82,052, herein after Kim) .

With respect to claim 1Rho describes a method of fabricating a liquid crystal display device, comprising : forming a thin film transistor in a pixel region (Rho figure 8 #50, col. 4 lines 64-65, Rho figure 2 # 21 –pixel, col. 5 lines34-36) and a pad on an edge region of a first substrate; (Rho figure 8 # 41,col. 7 lines 15-20) depositing an organic passivation layer over the first substrate; (Rho col. 7 lines 15-20) and removing

the organic passivation layer in the edge region using a diffraction mask to expose a portion of the pad, (Rho figure 5 and col. 6 lines 1-5, col. 3 lines 37-40) .

Rho does not specifically describe the diffraction mask having a slit portion including slits having a plurality of different widths.

However, Kim , a patent from the same filed of endeavor, describes in figure 28 and col. 3 lines 1 to 10, etc. the diffraction mask having a slit portion including slits having a plurality of different widths to provide data lines at opposite sides of the pixel areas so that variation in the pixel voltage due to the parasitic capacitance between partitioned areas with different degree of misalignment is reduced and pixel voltage variation between the two partitioned areas is reduced to prevent non-uniformity in the brightness.

Therefore it would have been obvious to use Kim's diffraction mask having a slit portion including slits having a plurality of different widths In Rho's masks, the motivation to include the above is " to provide data lines at opposite sides of the pixel areas so that variation in the pixel voltage due to the parasitic capacitance between partitioned areas with different degree of misalignment is reduced and pixel voltage variation between the two partitioned areas is reduced to prevent non-uniformity in the brightness." (Kim col. 3 lines 33-36 and 40-43).

With respect to claim 2 Rho describes the method of claim 1, wherein the organic passivation is formed of one of benzo cyclo butene (BCB) and photo- layer acryl. (Rho col. 5 lines 17-22, Kim col. 6 lines 49-50) .

With respect to claim 3 Rho to the extent understood, describes the method of claim 1, wherein the removing the organic passivation comprises, (Rho figures 5-8 ,e tc.) depositing a photoresist layer on the organic passivation layer in the edge region; (Rho figures 6-7 , col. 6 lines 11-20) placing the diffraction mask having first and second light transmission regions over the photoresist layer for a light exposure, (Kim figure 28) so that the first light transmission region transmits an amount of light greater than the second region; light transmission photoresist layer to (Kim it is inherent that a slit with wider width will transmit a greater amount of light) completely remove the photoresist layer of the second light transmission region and to remain the photoresist layer of the first light transmission region; (Rho figure 16 B) developing the etching the organic passivation layer to remove a part of the organic passivation layer of the second light transmission region; removing the photoresist layer; and etching the organic passivation layer to remove a remaining organic passivation layer. (Rho figs. 14b to 16B).

With respect to claim 4 Rho describes the method of claim 3, wherein the diffraction mask of the second transmission region has a slit width greater than that of the first transmission region. (Kim figure 28)

With respect to claim 5 , to the extent understood, Rho describes the method of claim 3, wherein the second light transmission region has the diffraction mask of a plurality of slits. (Kim figure 28)

With respect to claim 6 Rho to the extent understood, describes the method of claim 1, wherein the forming a thin film transistor comprises, forming a gate electrode on the first substrate; (Rho figs. 2-3 # 20 on 10, col. 4 line 62) insulating layer over the

first substrate; (Rho figs. 2,3 # 40, col. 4 line 49-50) depositing a gate forming a semiconductor layer on the gate insulating layer; (Rho figs, 2-3 # 20) and forming a source electrode and a drain electrode on the semiconductor layer. (Rho figs. 2-3 # 80,90, col. 4 lines 62-63),

With respect to claim 7 Rho describes the method of claim 1, further comprising forming a metal layer on the exposed portion of the pad. (Rho figure 8)

With respect to claim 8 Rho describes the method of claim 7, wherein the metal layer is formed of one of indium tin oxide (ITO) and indium zinc oxide (IZO). (Rho col. 3 line 46, kim col 6 lines 49-50) .

With respect to claim 9 Rho describes the method of claim 1, further comprising: forming a black matrix and a color filter layer on a second substrate; (Rho fig.13, col. 8 lines 10-22) forming a sealant on the edge region of the first substrate and attaching the first and second substrates to each other; and forming a liquid crystal layer between the first and second substrates. (Rho fig. 13 , Kim figures 1,2 col. 6 lines 55-60)

With respect to claim 10 Rho describes a method of fabricating a liquid crystal display device, comprising : forming a thin film transistor in a pixel region and a pad on an edge region of a first substrate; depositing an organic passivation layer over the first substrate; depositing a photoresist layer layer in the edge region; placing the diffraction mask having first and second light transmission regions over the photoresist layer for a light exposure, so that the first light transmission region transmits an amount of light greater than the second light transmission region; (rejected for same reasons as set out under claim 1 above) developing the photoresist layer to completely remove the

photoresist layer of the second light transmission region and to remain the photoresist layer of the first light transmission region ; etching the organic passivation layer to remove a part of the organic passivation layer of the second light transmission region ; removing the photoresist layer; and etching the organic passivation layer to remove a remaining organic passivation layer. (rejected for same reasons as set out under claim 3 above).

With respect to claim 11 Rho describes the method of claim 10, wherein the organic passivation layer is formed of one of benzo cyclo butene (BCB) and photo-acryl. (Rho col. 5 lines 17-22, Kim col. 6 lines 49-50) .

With respect to claim 12 Rho describes the method of claim 10, wherein the diffraction mask of the second transmission region has a slit width greater than that of the first transmission region. (Kim figure 8)

With respect to claim 13 Rho describes the method of claim 10, wherein the diffraction mask of the second light transmission region has a plurality of slits. (Rho and Kim figure 8) .

With respect to claim 14 to the extent understood, Rho describes the method of claim 10, wherein the forming a thin film transistor comprises, forming a gate electrode on the first substrate; depositing a gate insulating layer over the first substrate; forming a semiconductor layer on the gate insulating layer; and forming a source electrode and a drain electrode on the semiconductor layer. (rejected for reasons set out under claim 6 above).

With respect to claim 15 to the extent understood, Rho describes the method of claim 10, further comprising forming a metal layer on the exposed portion of the pad. (Rho figure 8, col. 3 lines 46-47)

With respect to claim 16 to the extent understood, describes the method of claim 15, wherein the metal layer is formed of one of indium tin oxide (ITO) and indium zinc oxide (IZO). (Rho col. 3 lines 46-47, Kim col. 6 lines 49-50).

With respect to claim 17 Rho to the extent understood, describes the method of claim 10, further comprising: forming a black matrix and a color filter layer on a second substrate; (Rho fig. 13, col. 8 lines 10-22) forming a sealant on the edge region of the first substrate and attaching the first and second substrates to each other; and forming a liquid crystal layer between the first and second substrates. (Rho fig. 13 , Kim figures 1,2 col. 6 lines 55-60).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

August 25, 2005.

LONG PHAM
PRIMARY EXAMINER